



Media Backgrounder

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RapidIO Technology Overview

RapidIO is a switch fabric control plane interconnect for the chips and boards used inside high-performance embedded, networking and communications devices. It offers greater bandwidth, scalability and reliability than current bus interconnects and provides a smooth migration path from existing PCI and CPU architectures. The parallel RapidIO interconnect specification is available today to industry professionals at no charge. A serial RapidIO specification will be released by the end of the year.

Based on a switch-fabric architecture, RapidIO has been enhanced to meet the needs of the embedded market for a reliable intra-system interconnect in devices built with leading-edge processors. It supports transmission rates from two to hundreds of thousands of Gigabits per second (Gb/s). RapidIO allows engineers to design high-performance systems with state-of-the-art technology that are compatible with legacy systems, to lower manufacturing costs and to shorten product development cycles.

RapidIO Technical Highlights

High-performance embedded systems often operate under stressful conditions with stringent requirements. RapidIO was created to address these critical design issues with a stable and scalable interconnect that provides a practical migration path for the high-performance systems of the next decade and beyond. As a result, it provides several benefits that are important to current design implementations and that will be vital to future systems:

Real-time Performance

- High Bandwidth

Real-time performance is the result of high throughput and low latency. As a fabric-based architecture, RapidIO connects all the chips and devices within a system directly to each other. It allows multiple transactions to occur concurrently and supports transmissions of hundreds of Gigabits per second. The availability of large amounts of aggregate bandwidth increases system performance hundreds of times over today's hierarchical bus interconnects.

- Low Latency

Packet headers are as small as possible in RapidIO to control overhead and are organized for fast, efficient assembly and disassembly. Consequently, latency, or the time between requesting a transaction and when it is actually started, is kept to a minimum.

- Deterministic Performance

Real-time performance also requires determinism and the ability to prioritize the passage order of the most important transactions to maintain Quality of Service. RapidIO offers multiple message priority levels to guarantee that the most important transmissions reach their destination, even under the most stressful conditions. RapidIO is a load-store based architecture, that enables point-to-point determinism.

Scalability and Flexibility

- Scalable Data Widths and Clock Frequencies

The data rate of each RapidIO link can be implemented in a variety of data widths and clock frequencies. Links of different frequencies can exist within a single system, yielding the greatest design flexibility and forward compatibility. RapidIO interconnects have the potential to evolve over time to support various segments of the embedded market, such as systems that communicate over optical or take advantage of future high speed signaling.

- Scalable Number of Devices

The communications bandwidth of the RapidIO switch fabric scales, or can increase

proportionally, with the number of attached devices. There is little interconnect degradation as new devices or peripherals are added to the system and there is no practical limit on the number of devices that can be added to a system designed with RapidIO

Reliability

- Hardware Error Detection and Correction

The RapidIO architecture was designed for reliability from the bottom up. It is the only major fabric interconnect that includes hardware error detection and correction services performed on each individual link in the data transfer path. A separate CRC algorithm is used to detect corruption in the header and data payload, and all control packets are sent redundantly inverted to ensure complete coverage.

- No Packets Dropped

In the event of a non-correctable error, the packet is resent so that no packets are ever lost. Packets can be stomped immediately on detection of a problem, reducing the time required to recover from errors.

- Guaranteed Forward Progress

The RapidIO architecture also guarantees forward progress of the information packets. Each packet makes its way through the switch fabric one link at a time. If any particular link is busy, the packet does not have to go back the way it came, as with bus architectures, but simply waits until the link becomes available.

Software Transparency

- Compatible with PCI Device Drivers

A major benefit of the RapidIO technology is software compatibility with existing applications on devices with typical load-store architecture. This includes the software access to microprocessor external interfaces and PCI device drivers. Only the low-level setup interface to the operating system needs to be aware of RapidIO and consequently software vendors do not need to rewrite their core system interface programs.

- **No Software Protocol Stack Required**
RapidIO does not need a software protocol message passing stack. This is another example of the RapidIO technology's inherent compatibility with legacy systems and application software.

Low Cost, Easily Embedded Speeds Time-to-Market

- **Small Silicon Foot Print**
The RapidIO interface can be implemented in a corner of a processor, reducing the real estate necessary for interconnect processing.
- **Low Pin Count**
RapidIO has a low pin count compared to existing microprocessor buses, such as the PowerPC bus, or to existing I/O buses, such as PCI. The serial release of RapidIO enables very low pin counts for extreme power and pin-sensitive designs, such as DSPs.
- **Compatible with Standard FPGAs**
Designed specifically as an embedded interconnect, RapidIO technology is compatible with standard CMOS devices and the more-efficient LVDS voltage I/O commonly used in field programmable devices. RapidIO interfaces can be deployed within a small portion of a modern FPGA device and multiple ports are possible in ASICs or microprocessor implementations. Combined, these attributes enable fast prototyping, low-cost manufacturing and reduced time-to-market for new products.

The RapidIO interconnect architecture also offers an optional distributed globally-shared memory protocol extension that is useful for symmetric multiprocessing and shared data structures. This enables both general purpose multiprocessing and distributed I/O processing to co-exist under the same protocol.

From Hierarchical Bus to Switch Fabric Architecture

For the past decade, bridged hierarchies of single-channel buses have become the standard technology for connecting processors and peripherals on circuit boards. Data and processing instructions travel across the bus in one direction, like cars down a single-lane street. This is acceptable if traffic is light and the cars are only capable of traveling at low speeds.

With the faster processors and heavier data flows inundating computers today, however, hierarchical buses, such as PCI, have reached their physical limits. Every new attempt to expand the bus

creates yet another design difficulty. The interconnect “inside the box” has become the bottleneck to designing next-generation systems.

To resolve these issues, switch fabrics are becoming a popular alternative to aging hierarchical bus designs. Like the fibers in a woven cloth, switch fabrics directly connect all the devices in a system to each other. Multiple devices can communicate concurrently rather than having to wait for the single channel to become available, and packets in this architecture are literally switched among the various channels. The result is a significant increase in bandwidth and transmission speeds with no degradation as new devices are added.

Specification Development and Future

RapidIO is an open standard governed by an industry body. It is based on technology initiated by Motorola and Mercury Computer Systems that was transferred to the trade association early in the development process. As with all industry standards, the specification continues to evolve and is being enhanced to meet new market criteria through the ongoing efforts of the RapidIO Technical Working Group. Members can propose changes or additions to the specification for consideration by the association’s members.

For more details on the RapidIO technology, see the RapidIO white paper, “An Embedded System Component Network Architecture,” Frequently Asked Questions (FAQs) and other support documents, all of which can be downloaded at www.rapidio.org.

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